UTO-NBL-54LA

Datasheet

2025

Version 01.01

Beyond the technology

Utovertek

VERSION HISTORY

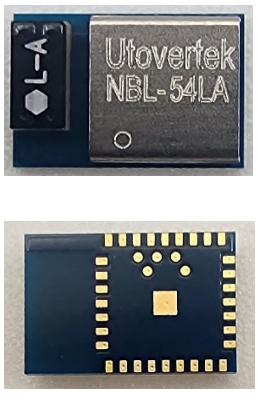
REVISION	AMENDMENT	DATE	
01.0	Initial version		
01.01	5.1 Layout Guide		

DESCRIPTION

UTO-NBL-54LA is a built-in Antenna Bluetooth Low Energy Module. UTO-NBL-54LA integrates all features of Bluetooth radio, software stack, GATT based profiles, antenna and host end user applications, which means no external micro controller. It provides a Bluetooth Low Energy fully compliant system for a data communication. At +8dBm TX Power and -96dBm RX Sensitivity UTO-NBL-54LA has best RF performance.

APPLICATION

- Commercial
- Sports and fitness
- Healthcare
- Medical sensors
- Home entertainment
- Mobile accessories
- Watch
- Human interface devices



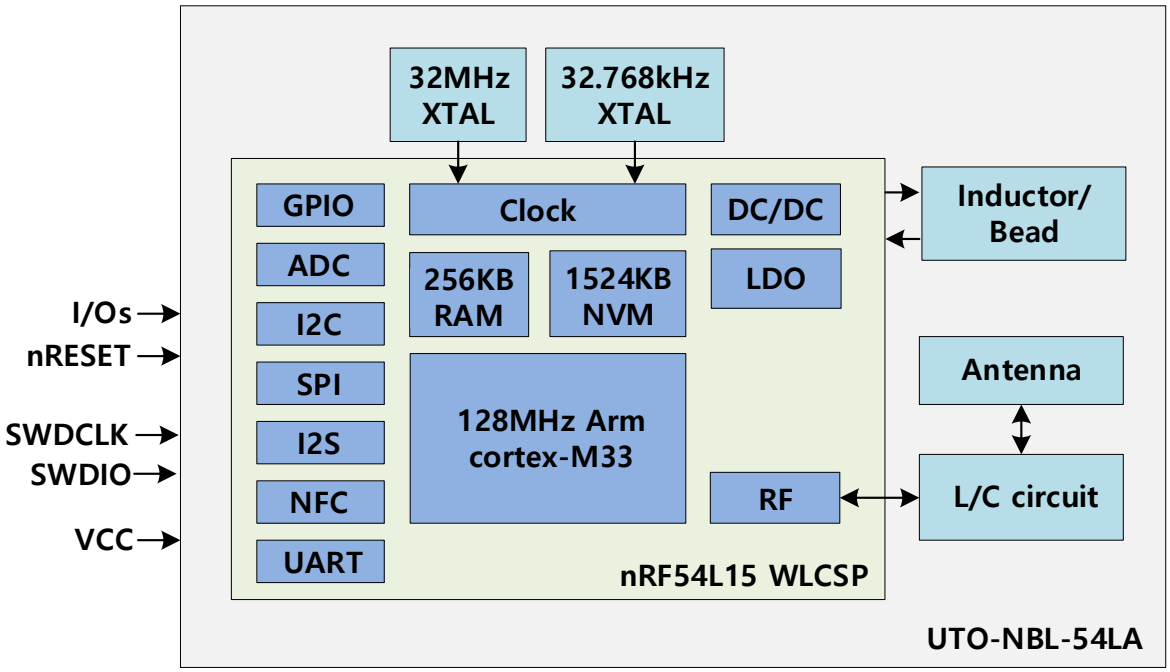
<Figure 1. UTO-NBL-54LA >

FEATURE

- nRF54L15 WLCSP
- Bluetooth v6.0 Single Mode Compliant
- Integrated Bluetooth Smart Stack
  . GAP, GATT, L2CAP and SMP
  . Bluetooth Smart profiles
- RF Performance
  . Transmit power : +8dBm (-8dBm ~ +8dBm)
  . Receiver sensitivity : -96dBm
- Low Power Consumption
  . Transmit : 4.8mA peak (0dBm)
  . Receiver : 3.4mA peak
  . Sleep mode : 0.6 uA (System OFF current)
- Peripheral Interfaces
  . UART/SPI(Master/Slave)/I2C
  . GPIO(30)
  . 14-bit ADC
  . I2S and PDM
  . Timer
  . Temperature Sensor
- Power supply : 1.7 ~ 3.6 V
- Dimension : 5.9 x 8.9 x 2.0mm (W x L x H)

1. Block Diagram

UTO-NBL-54LA's block diagram is illustrated in Figure 2 below.



<Figure 2. Simplified block diagram of UTO-NBL-54LA>

CPU and Memory

The Main core is **ARM Cortex-M33**. The processor has a 32-bit instruction set that implements a super set of 16- and 32-bit instructions to maximize code density and performance.

- Digital signal processing (DSP) instructions

  . Single-cycle multiply and accumulate (MAC) instructions

  . 8-and 16-bit single instruction multiple data (SIMD) instructions

- Hardware divide
- Single-precision floating-point unit (FPU)
- Memory Protection Unit (MPU)
- Arm TrustZone for Armv8-M
- Stack limit checking
- The Arm Cortex Microcontroller Software Interface Standard (CMSIS)
- Nested Vectored Interrupt Controller (NVIC)
- 256KB RAM
- 1524 NVM(RRAM)

Power management

UTO-NBL-54LA supports DC/DC mode. The module have Power Inductor and Ferrite bead coil for the DC/DC mode.

- Radio domain
- Peripheral domain (PERI)
- Low-power domain (LP)

Clock management

The module have a 32 MHz main crystal oscillator and 32.768 kHz RTC crystal oscillator.

Peripherals

The **comparator peripheral (COMP)** compares one input voltage (VIN+) against another input voltage (VIN-). VIN+ can be derived from an analog input pin (PIN0 to AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator.

- Input range from 0V to VCC
- Single-ended mode
- Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
- Configurable hysteresis
- Reference inputs (VREF)
- External reference from AIN0 to AIN7 (between 0V and VCC)
- Internal VCC reference
- 1.2V internal reference
- Two speed/power consumption modes, low-power and high-speed
- Single-pin capacitive sensor support
- Event generation on output changes
- UP event on VIN- > VIN+
- DOWN event on VIN- < VIN+
- CROSS event on VIN+ and VIN- crossing
- READY event on core and internal reference (if used) ready

The **general GPIO** is organized as one port with up to 30 I/Os enabling access and control of up to 30 pins through one port. Each GPIO can be accessed individually with the following user configurable features.

- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins in PERI and LP power domains
- Trigger interrupt on state changes on any pin on selected ports
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register
- Support for secure and non-secure attributes for pins in conjunction with the system protection unit

The **GPIO tasks and events (GPIOTE)** peripheral provides functionality for accessing GPIO pins using task and events. Each GPIOTE channel can be assigned to one pin.

- GPIO pin state change by triggering tasks
- Event generation on GPIO pin state change
- PORT event generation on GPIO DETECT signal
- Event generation on GPIO pin state change
- PORT event generation on GPIO DETECT signal
- Support for split security on individual GPIOTE channels

The **global real-time counter peripheral (GRTC)** is an ultra-low power shared system timer. GRTC implements a high-resolution system timer that is available in all power modes, including System

OFF. The system timer has a 1us resolution and 12 52 bits wide. This provides a run time of 142 years after initial power-on until the counter wraps around. It uses the 16MHz clock when the high-speed clock is active, but automatically switches to 32.768kHz in the other power modes. It will continue to be updated in all power modes. Due to the combination of clock sources, it has a 1us resolution and an accuracy equal to the 32.768kHz clock.

- System timer – SYSCOUNTER
- Pulse Width Modulation (PWM)
- Clock output on pin

The **I2S (Inter-IC Sound)** module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention. The I2S peripheral has the following main features :

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 32, 24, 16 and 8-bit sample width
- Separate sample and word widths
- Low-jitter Master Clock generator
- Various sample rates

The **low-power comparator (LPCOMP)** peripheral compares an input voltage against a reference voltage.

- Input range of 0 to VCC
- Ultra-low power
- Eight input options (AIN0 to AIN7)

- Two reference voltage options

  . Two external analog reference inputs

  . 15-level internal reference ladder (VCC/16)

- Optional hysteresis enable on input

- Wakeup source from System OFF or System ON sleep

The **Near field communication tag (NFCT)** peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

- NFC-A listen mode operation

  . 13.56MHz input frequency

  . Bit rate 106kbps

- Wake-on-field low power field detection (SENSE) mode

- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum

- Programmable frame timing controller

- Integrated automatic collision resolution, cyclic redundancy check (CRC), and parity functions

The **pulse density modulation (PDM)** module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (left and right) data input. Data is transferred directly to RAM buffers using EasyDMA.

- Up to two PDM microphones configured as a left/right pair using the same data input

- 8kHz, 16kHz, 32kHz, or 48kHz output sample rate, 16-bit samples.

- Supports digital microphone clocks at 768kHz, 800kHz, 1.024MHz, 1.536MHz, 2.048MHz, 3.072MHz, 1.28MHz and 2.56MHz

- Selectable ratio of 32, 48, 50, 64, 80, 96, 100 or 128 between PDM-CLK and output sample rate
- HW decimation filters
- EasyDMA support for sample buffering

The **pulse width modulation peripheral (PWM)** enables the generation of pulse width modulated signals on GPIO. The peripheral implements a counter with up-count mode and up-and-down-count mode, consisting of four PWM channels that can drive assigned GPIO pins.

- Programmable PWM frequency
- Up to four PWM channels with individual polarity and duty cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty cycle arrays (sequences) defined in RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA (no CPU involvement)
- Change of polarity, duty cycle, and base frequency on every PWM period
- RAM sequences can be repeated or connected into loops

The **Quadrature decoder (QDEC)** provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

- Digital wave form decoding from off-chip quadrature encoder
- Sample accumulation eliminating hard real-time requirements to be enforced on application
- Configurable sample period and accumulation to match application requirements
- Optional input de-bounce filters

- Optional LED output signal for optical encoders

The **2.4GHz radio transceiver (RADIO)** is compatible with multiple radio standards such as Bluetooth Low Energy, IEEE 802.15.4, and Nordic's proprietary protocols.

- Multidomain 2.4GHz radio transceiver, with

  . Bluetooth Low Energy 1 Mbps and 2 Mbps modes

  . Bluetooth Low Energy Long Range (125 kbps and 500 kbps) modes

  . IEEE 802.15.4 250 kbps mode

  . 1 Mbps, 2 Mbps and 4 Mbps Nordic proprietary modes

- Best in class link budget and low power operation
- Efficient data interface with EasyDMA support
- Automatic address filtering and pattern matching
- Automated packet assembler/disassembler
- Automated CRC generator and checker

The **Successive approximation analog-to-digital converter (SAADC)** is a differential successive approximation register (SAR) analog-to-digital converter.

- Four accuracy modes

  . 10-bit mode with a maximum sample rate of 2 Msps

  . 12-bit mode with a sample rate of 250 ksps

  . 14-bit mode with a sample rate of 31.25 ksps

  . Oversampling mode with configurable sample rate

- 10-bit resolution in single-ended mode, 11-bit resolution in differential mode, and 12/14-bit resolution with oversampling

- Multiple analog inputs

  . GPIO pins with analog function (input range 0 to VCC)

  . VCC (divided down to a valid range)

- Up to eight input channels

  . One input per single-ended channel, and two inputs per differential channel

  . Scan mode can be configured with both single-ended inputs and differential inputs

  . Each channel can be configured to select any of the above analog inputs

- Sampling triggered by a task from software or a DPPI channel for full flexibility on sample frequency source from low-power 32.768kHz RTC or more accurate 1/16MHz timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence with configurable sample delay
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit two's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- On-the-fly checking• Samples stored as 16-bit two's complement values for differential and single-ended sampling

The **Serial peripheral interface controller(SPIM)** with EasyDMA provides a full duplex, 4-wire synchronous serial communication interface.

- EasyDMA direct transfer to and from RAM
- SPI mode [0..3]
- Individual selection of I/O pins

- Optional D/CX output line for distinguishing between command and data bytes
- Optional hardware controlled chip select (CSN)

The **Serial peripheral interface(SPIS)** target with EasyDMA provides a full duplex, 4-wire synchronous serial communication interface.

- EasyDMA direct transfer to and from RAM
- SPI mode [0..3]
- Individual selection of I/O pins
- Hardware-based semaphore mechanisms for synchronizing access to data buffers by SPIS and CPU

The **temperature sensor (TEMP**) measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees
- TEMP analog electronics power down after temperature measurement is completed

The **Timer** peripheral is a general purpose timer allowing time intervals to be defined by user input.

- Two modes of operation: Timer mode and Counter mode
- Multiple capture/compare registers
- Compare event for every capture/compare registers
- 4-bit (1/2X) prescaler
- Configurable number of bits used by the TIMER: 8, 16, 24 or 32 bits

- TIMER runs on the high-frequency clock source (HFCLK)

The **two-wire interface controller peripheral (TWIM)** with EasyDMA provides a half duplex, two-wire synchronous serial communication interface which supports multiple targets in the same bus.

- I2C compatible for 100 kbps and 400 kbps
- 1000 kbps bit rate support for selected pull-up resistor/bus capacitance combinations
- Supported baud rate

  . 100 kbps, 400kbps, 1000kbps
- EasyDMA direct transfer to and from RAM
- Individual selection of I/O pins
- Support for clock stretching
- Transmissions can be suspended and resumed

The **two-wire interface target peripheral (TWIS)** with EasyDMA provides a half-duplex, two-wire synchronous serial communication interface.

- I2C compatible
- Supports 100 kbps and 400 kbps bit rate
- EasyDMA direct transfer to and from RAM
- Individual selection of I/O pins
- Support for clock stretching

The **Universal asynchronous receiver/transmitter (UARTE)** with EasyDMA peripheral provides a full-duplex, asynchronous serial communication interface with hardware flow control

- Full-duplex operation
- EasyDMA direct transfer to and from RAM
- Individual selection of I/O pins
- Slow instances with up to 1 Mbps baud rate
- Optional even and odd parity bit checking and generation
- One or two stop bits
- Configurable data frame size: 4 bit to 9 bit
- 9-bit mode support with address matching in RX
- Automatic hardware flow control
- Supports return to the IDLE state between transactions (when using HW flow control)
- Interrupt generation after programmable timeout

The **countdown Watchdog timer (WDT)** uses the low-frequency clock source(LFCLK) and offers configurable and robust protection against application lock-up

- Generates watchdog reset
- Optional pause of WDT when the CPU is sleeping or when it is stopped by the debugger
- Optional generation of non-maskable interrupt (NMI)
- Runs off the low-frequency clock source (LFCLK)

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage Temperature	-40	+125	Degree
VCC	-0.3	3.9	V
Other Terminal Voltages	-0.3	VCC+0.3	V

<Table 1 : Absolutes Maximum Ratings>

2.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature	-40	+85	Degree
VCC	1.7	3.6	V
VIH(Input High GPIO V)	0.7*VCC	VCC	V
VIL(Input Low GPIO V)	0	0.3*VCC	V

<Table 2 : Recommended Operating conditions>

2.3 Current consumption

Power mode	Condition	Min	Typ	Max	Unit
Transmit (DCDC, 3V)	Pout = 0 dBm		4.8		mA
Receive (DCDC, 3V)	At 1 Mbps		3.4		mA

<Table 3 : Current consumption>

2.4 RF Characteristics

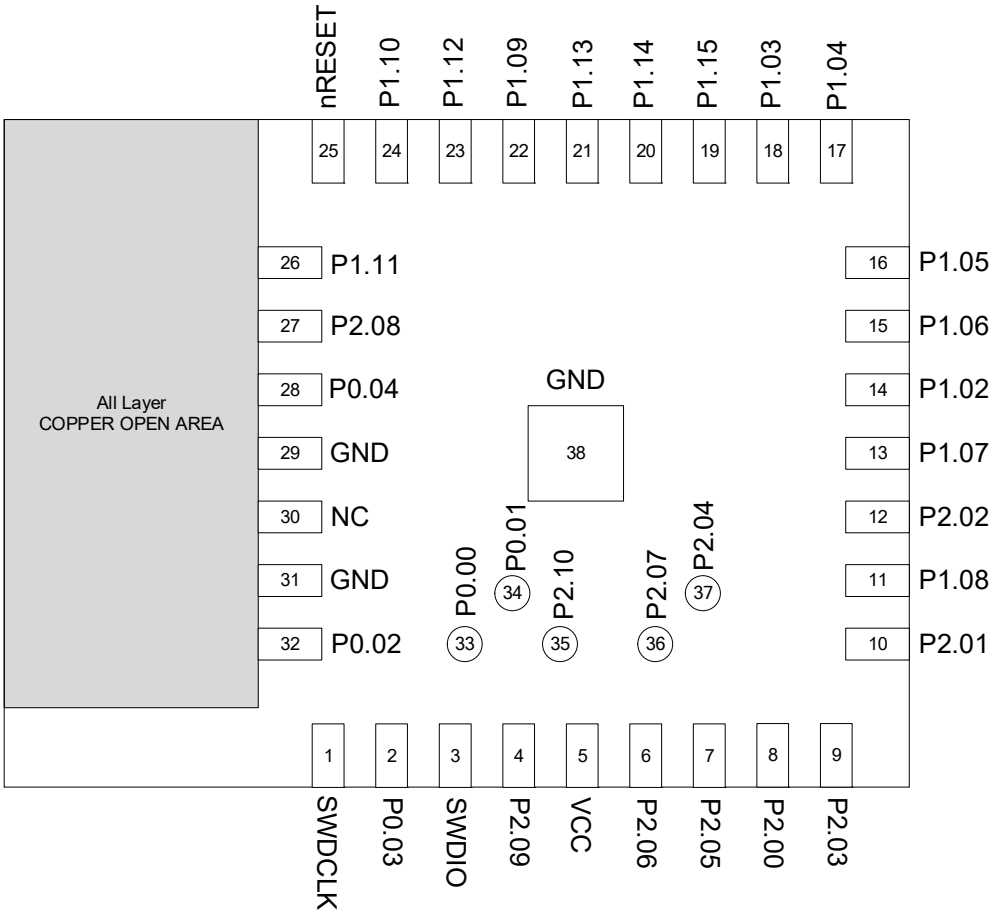
Rating	Min	Typ	Max	Unit
Operating frequencies	2360		2500	MHz
TX Maximum output power		8		dBm
TX RF power accuracy			+/-2	dB
TX Adjacent Channel Transmit Power 2MHz (1 Mbps)		-48		dBc
TX Adjacent Channel Transmit Power 3MHz (1 Mbps)		-54		dBc
TX Adjacent Channel Transmit Power 4MHz (2 Mbps)		-51		dBc
TX Adjacent Channel Transmit Power 6MHz (2 Mbps)		-56		dBc
RX maximum received signal strength at < 0.1% PER		0		dBm
RX Sensitivity (0.1% BER) at 2 Mbps		-90		dBm
RX Sensitivity (0.1% BER) at 1 Mbps		-93		dBm

<Table 4 : RF Characteristics>

3. Pin Description

UTO-NBL-54LA's PIN descriptions are summarized in Figure 3 and Table 5 below.

UNIT : mm



- Top View (Bottom pad)

<Figure 3. PIN descriptions>

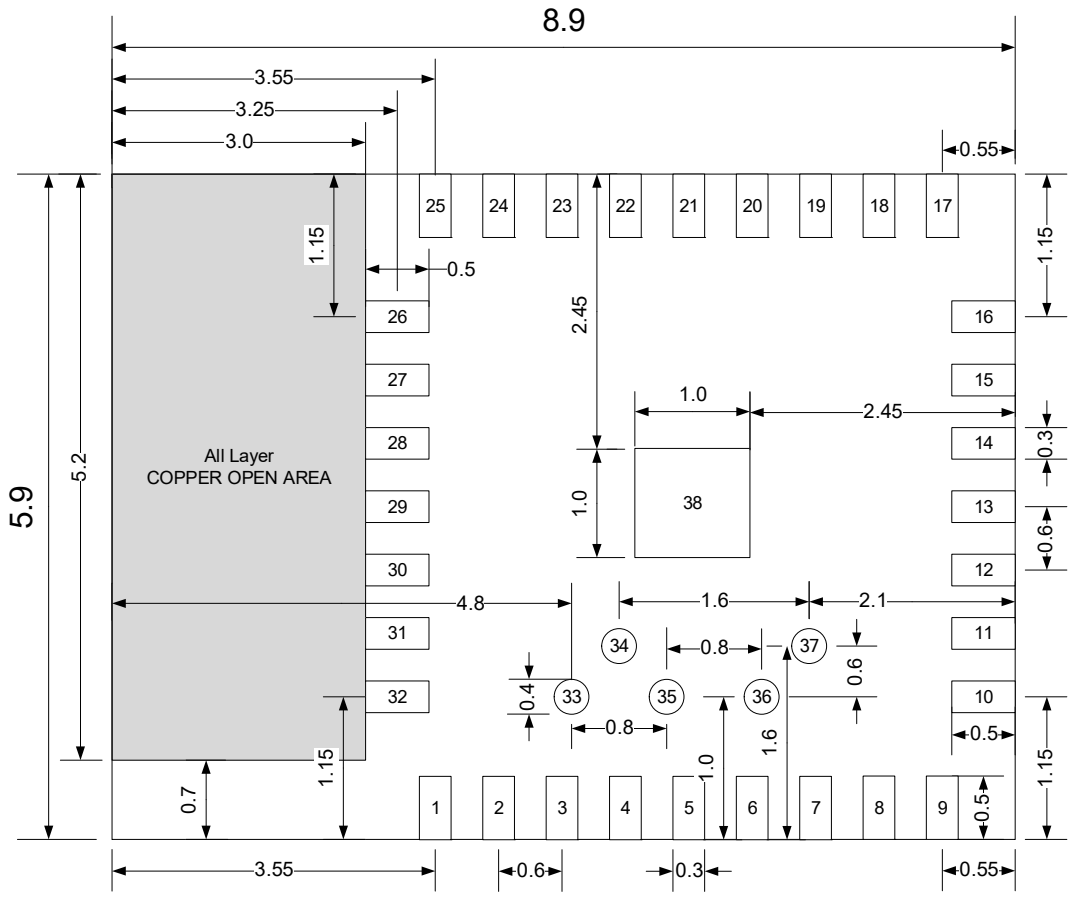
Num.	PIN Name	Type	Description
1	SWDCLK	Debug	Serial wire clock
2	P0.03	I/O	General purpose I/O GRTC PWM output
3	SWDIO	Debug	Serial wire data
4	P2.09	I/O	General purpose I/O Trace data 2 SPIM SDI (SPIN00/21) SPIS SDI (SPIS00/21) UARTE CTS (UARTE00/21)
5	VCC	Supply voltage	Power supply
6	P2.06	I/O	General purpose I/O SPIM SCK (SPIM00/21) SPIS SCK (SPIS20/21) Trace clock
7	P2.05	I/O	General purpose I/O SPIM CS (SPIM00/20) UARTE RTS (UARTE00/20) QSPI CS (FLPR)
8	P2.00	I/O	General purpose I/O SPIM DCX (SPIM00/20) UARTE RXD (UARTE00/20) QSPI D3 (FLPR)
9	P2.03	I/O	General purpose I/O QSPI D2 (FLPR)
10	P2.01	I/O	General purpose I/O SPIM SCK (SPIM00/20) SPIS SCK (SPIS00/20) QSPI SCK (FLPR)
11	P1.08	I/O	General purpose I/O GRTC HF clock output ADC external reference input (SAADC)
12	P2.02	I/O	General purpose I/O SPIM SDO (SPIM00/20) SPIS SDO (SPIS00/20) UARTE TXD (UARTE00/20) QSPI D0 (FLPR) Serial wire output (SWO)

13	P1.07	I/O	General purpose I/O TAMPC active shield 1 input AIN3 (analog input)
14	P1.02	I/O	General purpose I/O NFC antenna connection
15	P1.06	I/O	General purpose I/O TAMPC active shield 1 output AIN2 (analog input)
16	P1.05	I/O	General purpose I/O TAMPC active shield 0 input RADIO DFEGPIO AIN1 (analog input)
17	P1.04	I/O	General purpose I/O TAMPC active shield 0 output AIN0 (analog input)
18	P1.03	I/O	General purpose I/O NFC antenna connection
19	P1.15	I/O	General purpose I/O
20	P1.14	I/O	General purpose I/O RADIO DFEGPIO AIN7 (analog input)
21	P1.13	I/O	General purpose I/O RADIO DFEGPIO AIN6 (analog input)
22	P1.09	I/O	General purpose I/O TAMPC active shield 2 output RADIO DFEGPIO
23	P1.12	I/O	General purpose I/O. TAMPC active shield 3 input RADIO DFEGPIO AIN5 (analog input)
24	P1.10	I/O	General purpose I/O TAMPC active shield 2 input RADIO DFEGPIO
25	nRESET	Reset	Reset active low with on-chip pull-up
26	P1.11	I/O	General purpose I/O TAMPC active shield 3 output RADIO DFEGPIO

			AIN4 (analog input)
27	P2.08	I/O	General purpose I/O Trace data 1 SPIM SDO (SPIN00/21) SPIS SDO (SPIS00/21) UARTE TXD (UARTE00/21)
28	P0.04	I/O	General purpose I/O GRTC LF clock output
29	GND	GND	Ground
30	NC	NC	NC
31	GND	GND	Ground
32	P0.02	I/O	General purpose I/O
33	P0.00	I/O	General purpose I/O
34	P0.01	I/O	General purpose I/O
35	P2.10	I/O	General purpose I/O Trace data 3 SPIM CS (SPIM00/21) UARTE RTS (UARTE00/21)
36	P2.07	I/O	General purpose I/O Trace data 0 SWO (serial wire output) SPIM DCX (SPIM00/21) UARTE RXD (UARTE00/21)
37	P2.04	I/O	General purpose I/O SPIM SDI (SPIM00/20) SPIS SDI (SPIS00/20) UARTE CTS (UARTE00/20) QSPI D1 (FLPR)
38	GND	GND	Ground

4. Physical Dimensions

UNIT : mm



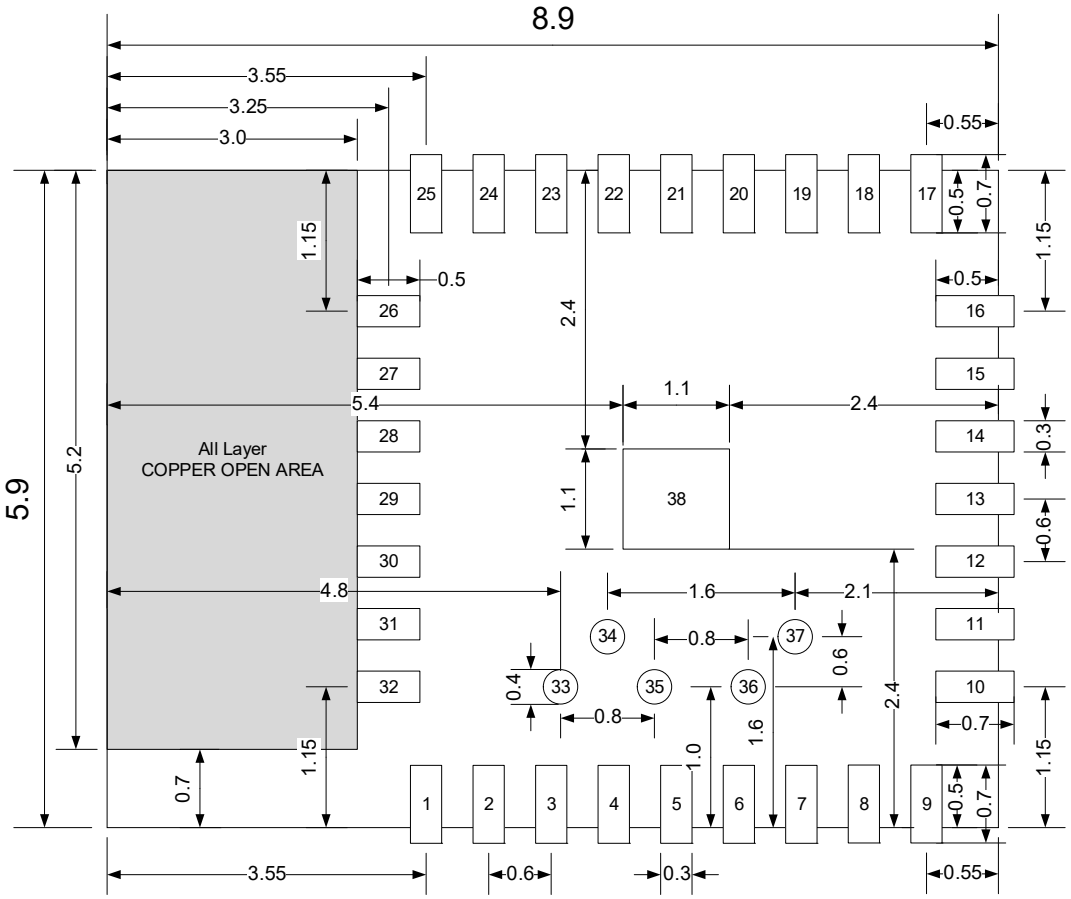
33,34,35,36,37 PAD : 0.4Ø

- Top View (Bottom pad)

<Figure 4. Physical dimension>

5. Layout

UNIT : mm



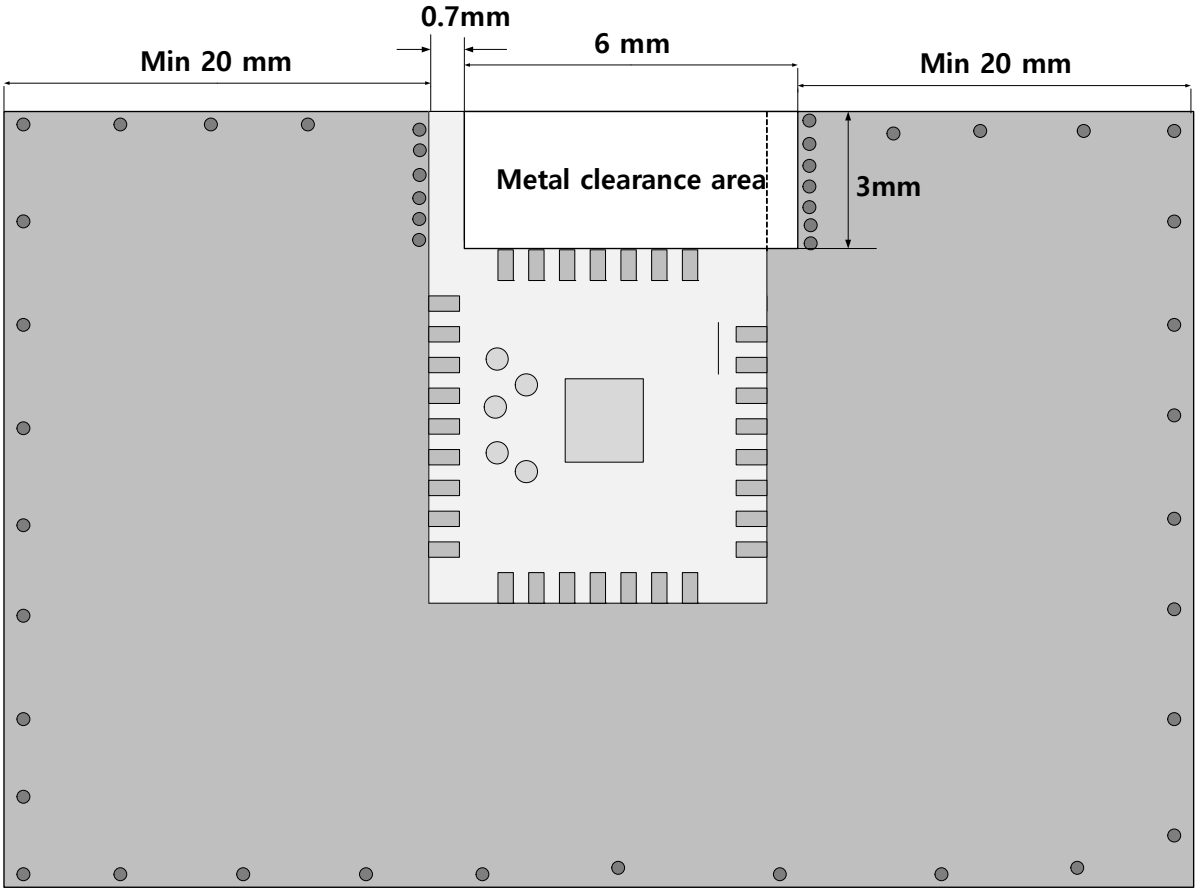
33,34,35,36,37 PAD : 0.4∅

- Top View (Bottom pad)

<Figure 5. Layout>

5.1 Layout Guide

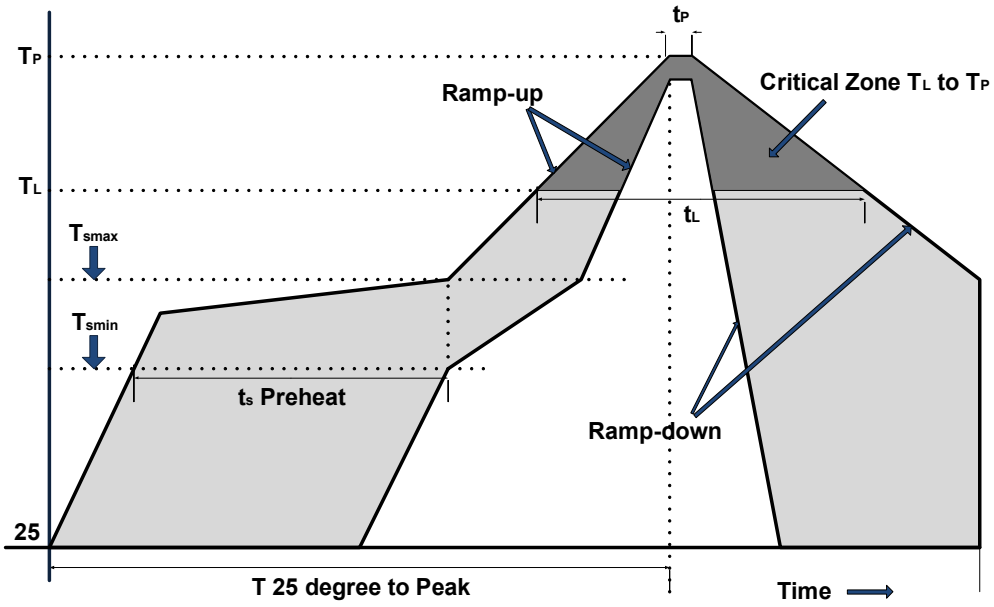
To achieve best radio performance for UTO-NBL-54LA, it is recommended to use the module at the edge of the PCB as shown in Figure 6. Do not place any metal (traces, components, etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Do not place plastic or any other dielectric material in touch with the antenna.



<Figure 6. Recommended layout>

6. Re-flow Temperature time profile

The data here is given only for guidance on solder and has to be adapted to your process and other re-flow parameters for example the used solder paste. The paste manufacturer provides a re-flow profile recommendation for his product.



<Figure 7. Soldering Temperature time profile>

Preheat		Main Heat		Peak	
Tsmax		TLmax		tpmax	
Temperature	Time	Temperature	Time	Temperature	Time
Degree	sec	Degree	sec	Degree	sec
150	100	217	90	260	10
		230	50		
Parameter				Value	Unit
Average ramp-up rate				3	Degree/sec
Average ramp-down rate				6	Degree/sec
Max. Time 25 degree to Peak Temperature				8	Min.

<Table 6 : Soldering temperature parameters>

Opposite side re-flow is prohibited due to module weight. Devices will withstand the specified profile and will withstand up to 1 re-flows to a maximum temperature of 260 degree. The re-flow soldering profile may only be applied if the UTO-NBL-54LA resides on the PCB side looking up. Heat above the solder eutectic point while the UTO-NBL-54LA is mounted facing down may damage the module permanently.

7. Certification

7.1 Bluetooth SIG Listing

7.2 FCC

7.3 CE

7.4 KC

7.5 IC

7.6 JPMIC (JAPAN)

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